AMENDMENTS TO THE CLAIMS

Claims 1-2 (Cancelled)

3. (Previously Presented) A semiconductor circuit comprising:

a first transistor having:

a first semiconductor region;

spaced-apart source and drain regions formed in the first semiconductor region;

a first channel defined between the source and drain regions, the first channel having a first channel length and a first dopant concentration;

a layer of first gate oxide formed over the first channel, the layer of first gate oxide having a thickness; and

a gate formed over the layer of first gate oxide;

the first transistor conducting more than a leakage current when the gate, the source, and the first semiconductor region are connected to a same potential;

a second transistor having:

a second semiconductor region;

spaced-apart source and drain regions formed in the second semiconductor region;

a second channel defined between the source and drain regions formed in the second semiconductor region, the second channel having a second channel length and a second dopant concentration;

a layer of second gate oxide formed over the second channel, the layer of second gate oxide having a thickness, the thickness of the layer of first gate oxide being substantially less than the thickness of the layer of second gate oxide; and

a gate formed over the layer of second gate oxide;

the second transistor being substantially non-conductive when the gate of the second transistor, the source of the second transistor, and the second semiconductor region are connected to a same potential, the first channel length being approximately 30 percent to 80 percent as long as the second channel length; and

a third transistor formed in the semiconductor material, the third transistor having a third channel and a layer of third gate oxide formed over the third channel, the third channel having a third channel length and a third dopant concentration, the layer of third gate oxide having a thickness, the third transistor being substantially non-conductive when zero volts are applied to the gate, the thickness of the layer of third gate oxide being substantially equal to the thickness of the layer of first gate oxide.

4. (Original) The circuit of claim 3 wherein the first dopant concentration is substantially equal to a sum of the second dopant concentration and a dopant concentration implanted into the third channel.

5. (Original) The circuit of claim 4 wherein the second and third transistors have source and drain regions of the same conductivity type, and the first transistor has source and drain regions of an opposite conductivity type.

6. (Original) The circuit of claim 4 wherein the first and third transistors have source and drain regions of the same conductivity type, and the second transistor has source and drain regions of an opposite conductivity type.

7. (Previously Presented) The circuit of claim 3 wherein the source and drain regions of the second transistor are spaced apart from the source and drain regions of the first transistor.

8. (Previously Presented) The circuit of claim 3 wherein the gate formed over the layer of second gate oxide does not contact the source or drain region of the second transistor.

9. (Previously Presented) The circuit of claim 10 wherein the first channel length is approximately 30 percent to 80 percent as long as the second channel length.

Claims 10-14 (Cancelled)

15. (New) A semiconductor circuit comprising:

a first transistor having:

a first semiconductor region;

spaced-apart first source and drain regions that contact the first semiconductor region, the first source and drain regions and the first semiconductor region having opposite conductivity types;

a first channel region that contacts and lies between the first source and drain regions, the first channel region having a first channel length;

a layer of first gate oxide formed over the first channel region, the layer of first gate oxide having a first thickness; and

a first gate that contacts the layer of first gate oxide and lies over the first channel region;

the first transistor conducting more than a leakage current when the first gate, the first source, and the first semiconductor region are connected to a same potential;

a second transistor having:

a second semiconductor region;

spaced-apart second source and drain regions that contact the second semiconductor region, the second source and drain regions and the second semiconductor region having opposite conductivity types;

a second channel region that contacts and lies between the second source and drain regions, the second channel region having a second channel length that is greater than the first channel length;

a layer of second gate oxide formed over the second channel region, the layer of second gate oxide having a second thickness that is greater than the first thickness; and

a second gate that contacts the layer of second gate oxide and lies over the second channel region;

the second transistor being substantially non-conductive when the second gate, the second source, and the second semiconductor region are connected to a same potential.

16. (New) The circuit of claim 15 and further comprising a third transistor, the third transistor having:

a third semiconductor region;

spaced-apart third source and drain regions that contact the third semiconductor region, the third source and drain regions and the third semiconductor region having opposite conductivity types;

a third channel region that contacts and lies between the third source and drain regions;

a layer of third gate oxide formed over the third channel region; and

a third gate that contacts the layer of third gate oxide and lies over the third channel region;

the third transistor being substantially non-conductive when the third gate, the third source, and the third semiconductor region are connected to a same

potential, the first channel region having a dopant concentration substantially equal to a sum of a dopant concentration of the second channel region and a dopant concentration of the third channel region.

17. (New) The circuit of claim 16 wherein the dopant concentration of the second channel region and the dopant concentration of the third channel region are different.

18. (New) The circuit of claim 16 wherein the second semiconductor region and the third semiconductor region have a same conductivity type.

19. (New) The circuit of claim 16 wherein the second semiconductor region and the third semiconductor region have an opposite conductivity type.

20. (New) The circuit of claim 16 wherein the first semiconductor region and the third semiconductor region have a same conductivity type.

21. (New) The circuit of claim 16 wherein the first semiconductor region and the third semiconductor region have an opposite conductivity type.

22. (New) The circuit of claim 15 wherein the second channel length is substantially greater than the first channel length.

23. (New) The circuit of claim 22 wherein the second thickness is substantially greater than the first thickness.

24. (New) The circuit of claim 15 wherein the second thickness is substantially greater than the first thickness.